WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor integrated circuit device, comprising:

providing a semiconductor substrate with an active region defined by an element isolation region, word lines extending in a first direction over said active region such that gate electrodes of metal insulator semiconductor field effect transistors (MISFETs) are electrically coupled to said word lines, semiconductor regions formed in said active region such that said semiconductor regions serve as a source region or a drain region of each MISFET;

forming a first insulating film over said active region, said word lines and said semiconductor regions;

forming a first opening in said first insulating film such that said first opening is arranged between said word lines and extends, in said first direction, from a semiconductor region to said element isolation region;

forming a second opening in said first insulating film under said first opening such that, in said first direction, a diameter of said first opening is less than that of said second opening and such that said second opening reaches said semiconductor region;

burying a conductive material in said first opening and in said second opening; and

forming a bit line over said first insulating film such that said bit line is electrically coupled to said conductive material and extends to cross said word lines.

2. A method according to claim 1, further comprising:

forming a capacitor element over said first insulating film,

wherein, during said second opening forming step, a third opening is formed to reach other semiconductor region,

wherein, during said conductive material burying step, a conductive material is buried in said third opening, and

wherein said capacitor element is electrically coupled to said other semiconductor region through said conductive material buried in said third opening.

3. A method according to claim 2, wherein, during said first opening forming step, a portion where said third opening is to be formed is not etched.

4. A method according to claim 2, wherein a memory cell of a dynamic random access memory is comprised of said MISFET and said capacitor element.

5. A method of manufacturing a semiconductor integrated circuit device, comprising:

providing a semiconductor substrate with an active region defined by an element isolation region, a gate electrode of a metal insulator semiconductor field effect transistor (MISFET) and semiconductor regions formed in said active region such that said semiconductor regions serve as a source region or a drain region of each MISFET;

forming a first insulating film over said active region and said semiconductor regions;

forming a first opening in said first insulating film such that said first opening extends, in a first direction, from a semiconductor region to said element isolation region; and

forming a second opening in said first insulating film under said first opening such that, in said first direction, a diameter of said first opening is less than that of said second opening and such that said second opening reaches said semiconductor region,

wherein, in said second opening forming step, a third opening is formed to reach the other semiconductor region,

wherein, in said first opening forming step, a portion where said third opening is to be formed is not etched; and

wherein a conductive material is buried in said first, second, third openings.

6. A method according to claim 5, further comprising:

forming a bit line over said first insulating film such that said bit line is electrically coupled to said conductive material buried in said first and second openings;

forming a capacitor element over said first insulating film such that said capacitor element is electrically coupled to other semiconductor region through said conductive material buried in said third opening.

7. A method according to claim 6, wherein a memory cell of a dynamic random access memory is comprised of said MISFET and said capacitor element.

8. A method of manufacturing a semiconductor integrated circuit device, comprising:

providing a semiconductor substrate with an active region defined by an element isolation region, a gate electrode of a metal insulator semiconductor field effect transistor (MISFET) and semiconductor regions formed in said active region such that said semiconductor regions serve as a source region or a drain region of each MISFET;

forming a first insulating film over said active region and said semiconductor regions;

forming a first opening in said first insulating film such that said first opening extends, in a first direction, from a semiconductor region to said element isolation region;

forming a second opening in said first insulating film such that said second opening reaches said semiconductor region; and

burying a conductive material in said first, second, third openings,

wherein said second opening is formed under said first opening such that, in said first direction, a diameter of said first opening is less than that of said second opening and such that said second opening reaches said semiconductor region,

wherein, in said second opening forming step, a third opening is formed to reach other semiconductor region,

wherein, in said first opening forming step, a portion where said third opening is to be formed is not etched.

9. A method according to claim 8, further comprising:

forming a bit line over said first insulating film such that said bit is electrically coupled to said conductive material buried in said first and second openings; and

forming a capacitor element over said first insulating film such that said capacitor element is electrically coupled to the other semiconductor region through said conductive material buried in said third opening.

10. A method according to claim 9, wherein a memory cell of a dynamic random access memory is comprised of said MISFET and said capacitor element.

11. A semiconductor integrated circuit device, comprising:

a semiconductor substrate with an active region defined by an element isolation region, word lines extending in a first direction over said active region such that gate electrodes of metal insulator semiconductor field effect transistors (MISFETs) are electrically coupled to said word lines, semiconductor regions formed in said active region such that said semiconductor regions serve as a source region or a drain region of each MISFET;

a first insulating film covering said active region, said word lines and said semiconductor regions;

a first opening formed in said first insulating film such that said first opening is arranged between said word lines and extends, in said first direction, from a semiconductor region to said element isolation region;

a second opening formed in said first insulating film under said first opening such that, in said first direction, a diameter of said first opening is less than that of said second opening and such that said second opening reaches said

semiconductor regions;

a conductive material buried in said first opening and in said second opening; and

a bit line formed over said first insulating film such that said bit line is electrically coupled to said conductive material and extends to cross said word lines.

12. A semiconductor integrated circuit device according to claim 11, further comprising:

a capacitor element formed over said first insulating film;

a third opening formed in said first insulating film to reach other semiconductor region; and

a conductive material buried in said third opening,

wherein said capacitor element is electrically coupled to the other semiconductor region through said conductive material buried in said third opening.

13. A semiconductor integrated circuit device according to claim 12, wherein a memory cell of a dynamic random access memory is comprised of said MISFET and said capacitor element.